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Claims

[c1] A method of forming a PMOSFET comprising the steps of:
providing an SOI wafer having a buried insulator layer and a SOI layer above said buried insulator layer;
forming a layer of gate insulator over said SOI layer;
forming a transistor gate over said SOI layer having a channel underneath said gate;
forming insulator sidewalls on first and second sides of said gate;
epitaxially forming a doped layer containing a dopant on said SOI layer and adjacent to said insulator sidewalls;
diffusing said dopant into said SOI layer from said doped layer, thereby producing compressive stress in the horizontal direction parallel to an SOI surface and tensile stress in a vertical direction normal to said SOI surface in said channel; and
completing said PMOSFET.

[c2] A method according to claim 1, in which said step of diffusing is effected by a high temperature anneal.

[c3] A method according to claim 1, in which said step of diffusing continues until said germanium reaches a bottom

surface of said SOI layer.

[c4] A method according to claim 1, in which said step of diffusing stops before said germanium reaches a bottom surface of said SOI layer.

[c5] A method according to claim 1, in which said doped layer is SiGe.

[c6] A method according to claim 3, in which said dopant layer is SiGe with a Germanium concentration of greater than atomic number 20%..

[c7] A method according to claim 1, further comprising growing a layer of thermal oxide on said doped layer, thereby diffusing said dopant in the doped layer into said SOI layer.

[c8] A method according to claim 7, further comprising a step of removing said thermal oxide after said step of diffusing said dopant.

[c9] A method according to claim 7, in which said step of diffusing continues until said germanium reaches a bottom surface of said SOI layer.

[c10] A method according to claim 7, in which said step of diffusing stops before said dopant reaches a bottom surface of said SOI layer.

[c11] A method according to claim 7, in which said doped layer is SiGe.

[c12] A method according to claim 11, in which said doped layer is SiGe with a germanium concentration of greater than atomic number 20%.

[c13] A method of forming a PMOSFET comprising the steps of:
providing a bulk silicon wafer;
forming a layer of gate insulator over said bulk silicon;
forming a transistor gate over said bulk silicon having a channel underneath said gate;
forming insulator sidewalls on first and second sides of said gate;
epitaxially forming a doped layer containing germanium or impurity on said bulk silicon and adjacent to said insulator sidewalls;
diffusing germanium into said bulk silicon from said germanium doped layer, thereby producing compressive stress in horizontal direction (parallel to SOI surface) and tensile stress in vertical direction (in normal of SOI surface) in said channel; and
completing said PMOSFET.

[c14] A method according to claim 13, in which said step of

diffusing is effected by a high temperature anneal.

[c15] A method according to claim 13, in which said doped layer is SiGe.

[c16] A method according to claim 13, in which said dopant layer is SiGe with a germanium concentration of greater than atomic number 20%..

[c17] A method according to claim 13, further comprising growing a layer of thermal oxide on said dopant layer, thereby diffusing said dopant into said bulk silicon.

[c18] A method according to claim 17, further comprising a step of removing said thermal oxide after said step of diffusing said dopant.

[c19] A method according to claim 17, in which said dopant layer is SiGe.

[c20] A method according to claim 19, in which said dopant layer is SiGe with a germanium concentration of greater than atomic number 20%.

[c21] An integrated circuit containing at least one PMOSFET formed in an SOI wafer having a buried insulator layer and a SOI layer above said buried insulator layer;
said at least one PMOSFET having a gate insulator over said SOI layer;

a transistor gate over said SOI layer having a channel underneath said gate, said channel having compressive stress in the horizontal direction parallel to an SOI surface and tensile stress in a vertical direction normal to said SOI surface in said channel; and
wherein said SOI layer has a graded concentration of a dopant that generates said compressive stress in said horizontal direction, said concentration of said dopant having a maximum value at an upper surface of said SOI layer.

[c22] An integrated circuit according to claim 21, in which said graded concentration of dopant extends to a dopant depth less than a thickness of said SOI layer.

[c23] An integrated circuit according to claim 22, in which said SOI layer is silicon and said dopant is Germanium.

[c24] An integrated circuit according to claim 22, in which said graded concentration is formed by a high temperature anneal.

[c25] An integrated circuit according to claim 22, in which said graded concentration is formed by thermally oxidizing a deposited dopant layer disposed above said SOI layer.